IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Franciscus J. Klosters
Application No.: 10/590,405
Filed: October 30, 2007
For: ELECTRONIC CIRCUIT ARRANGEMENT FOR DETECTING A FAILING CLOCK

Group Art Unit: 2113
Examiner: Guyton, Philip A.
Confirmation No.: 8682

DECLARATION UNDER 37 C.F.R. 1.131

I, Franciscus J. Klosters, hereby declare that:

1. I am the sole inventor in U.S. Patent Application No. 10/590,405 ("the '405 Application") (U.S. Pat. Publ. No. 2008/0140890 A1);
2. Exhibit A attached herewith is an Invention Description dated December 2, 2003, which is evidence of conception of the subject matter described and claimed in the '405 Application at least as of December 2, 2003;
3. Exhibit B attached herewith is an ID Abstract dated December 18, 2003, regarding the ongoing preparation and review of the '405 Application; and
4. Exhibit C attached herewith is a Search Report dated December 22, 2003, regarding the ongoing preparation and review of the '405 Application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signed: _____ Date: 10-dec-2009

Franciscus J. Klosters
Gerstweg 2
6534 AE Nijmegen, NL